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INFORMATION SHEET

Title	Glass chip design guide

1 Summary

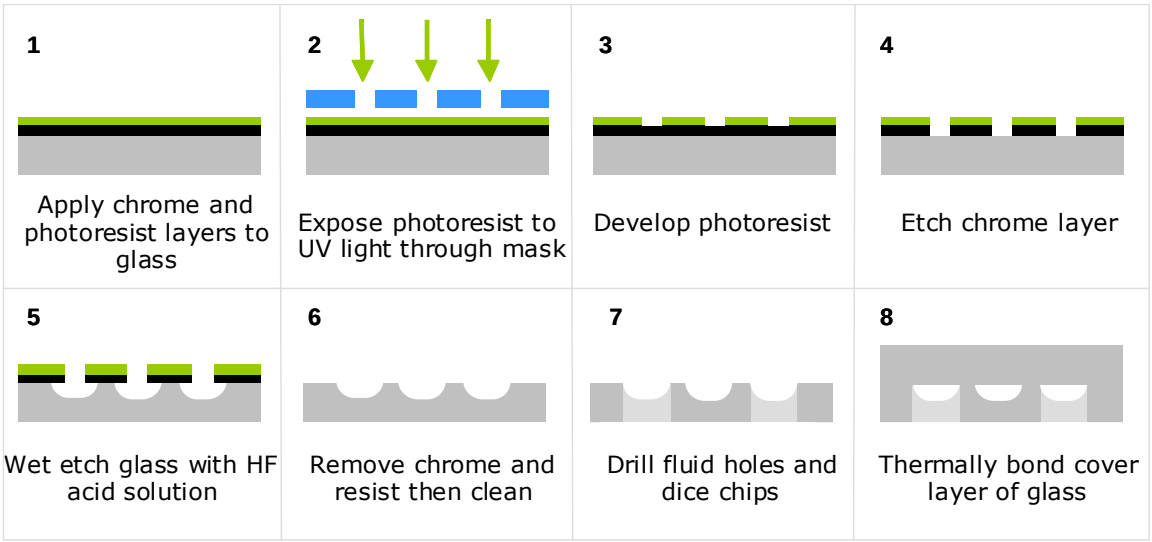
This document provides information required to design a glass microfluidic device with isotropically etched channels. This includes a summary of the fabrication process, a description drawing file formats that can be used and also some guidelines on how to design a chip that will work with standard Dolomite connectors.

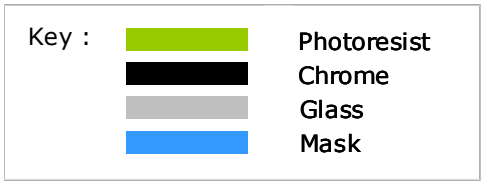
The processes apply to the fabrication of quartz (fused silica) chips with a few exceptions.

For information on Deep Reactive Ion Etching (DRIE) or polymer chip fabrication, please contact Dolomite.

2 Fabrication processes

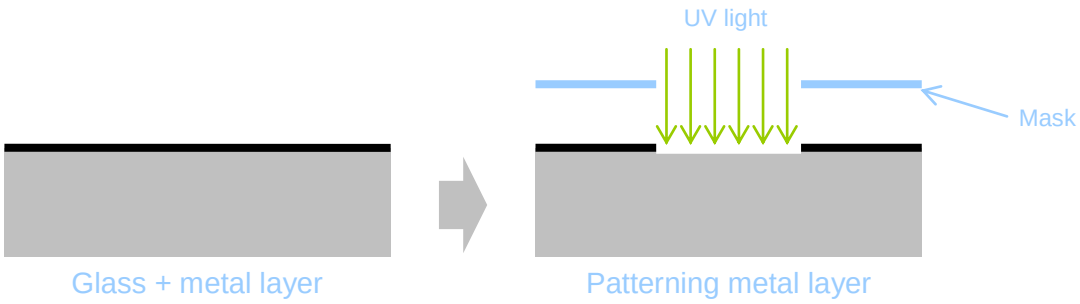
2.1 Fabrication process summary



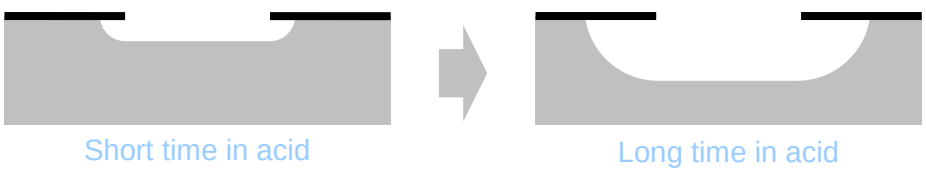


2.2 Isotropic etching

Isotropic or wet etching is used to form micro-channels and micro wells in glass wafers. To create a channel pattern a thin metal layer is first deposited on the glass surface. A photolithographic process is then used to create the pattern. A cross sectional view of this process is shown below:

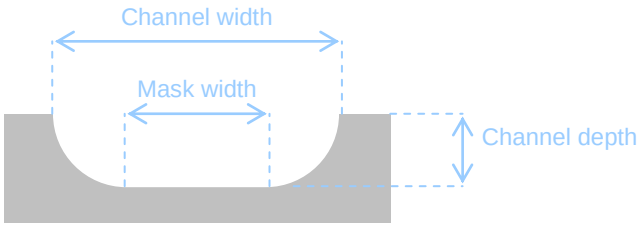


Hydrofluoric acid is then used to etch the exposed glass areas. The acid etches the glass all directions as shown below:



The etched surface is very smooth, similar to a polished surface (<5nm roughness).

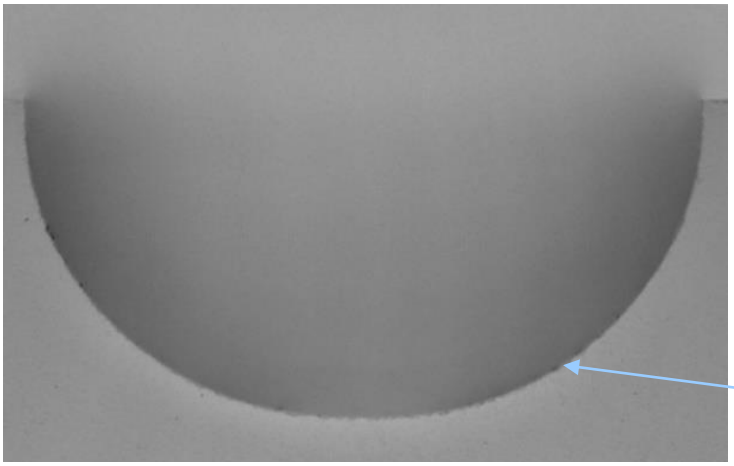
The metal layer is then removed. The resulting geometry is shown below:



Channel width = Mask width + 2 x Channel depth

Etch depth range = 0.25µm - 500µm

Minimum mask width = 10µm (or down to 1µm with a specialised mask)



Roughness occurred during dicing process (surface roughness from isotropic etching is <5nm)

Channel etched to 250 microns depth

2.3 Drilling holes

Prior to fusing the two glass layers fluid ports are drilled into one or both of the glass layers. The holes have parallel walls and are accurately aligned with the ends o the etched channels as shown below:

Drilled fluid ports

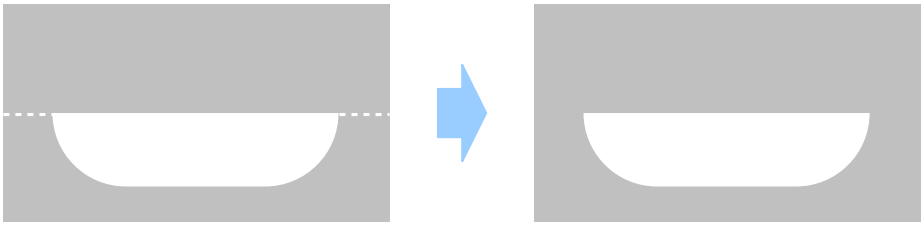
Hole diameter typically varies between 0.2m – 10mm in diameter.

2.4 Glass layer thickness

The standard glass layer thickness used for fabrication is 2mm. Standard chips therefore have a total thickness of 4mm. Thinner glass layers are possible with the minimum layer thickness around 50µm. Thicker glass layers are also possible.

2.5 Fusing process

To make a sealed microchannel a second glass layer is fused to the etched layer as shown below:



Top glass layer assembled

Thermally fuse layers

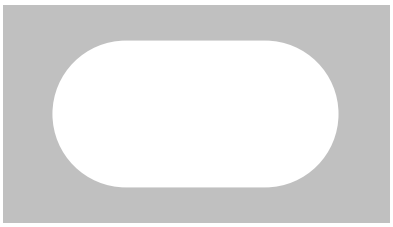
The thermal fusing process results in the two glass layers becoming one piece of glass. No adhesives or chemicals are required in this process. Once bonded glass devices can withstand pressures up to 300 Bar (standard connectors have a lower pressure rating).

2.5.1 Cold bonding

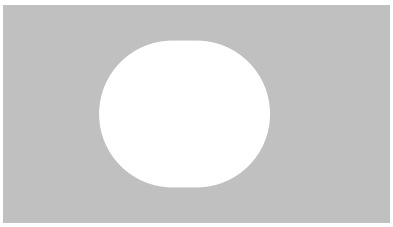
Cold bonding occurs when the two glass layers are brought into contact without heat. The flatness of the glass surfaces results in strong Van der Waals forces that hold the glass layers rigidly together. T-junction chips that have been fabricated using this process have withstood pressures up to 50 bar.

2.5.2 Fusing two etched layers

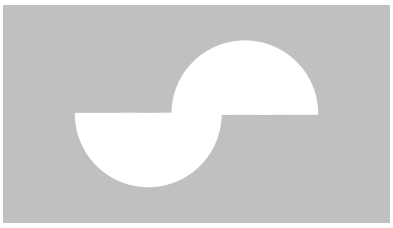
Microchannels are often etched into both glass surfaces to increase channel depth or to enable more complex geometries. Some examples are shown below:



Channel depth increased by a factor of two



Near circular channels can be formed with a narrow mask line



Channels may be offset; examples include micro-mixers and immiscible fluid contacting

Fluid paths with two different channel depths, examples include flow restrictors and filters

The standard alignment accuracy between layers is +/-5 µm. This can be improved upon on request (+/-2 µm).

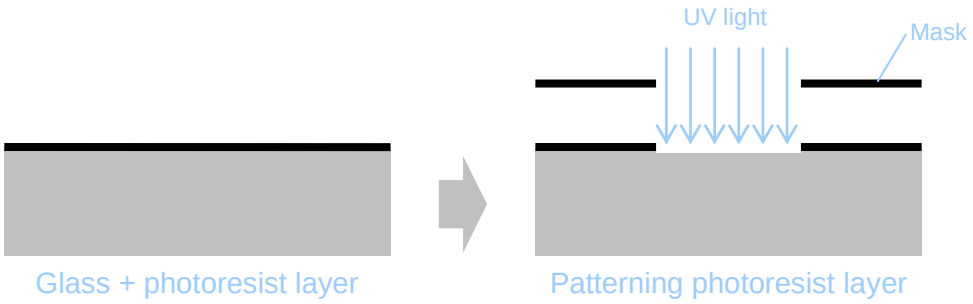
2.5.3 Multiple layer chips

Multiple glass layers can be fused to create more complex geometry as shown below:

Three layers of glass are fused on a regular basis but there is no limit in the number of layers that are possible. The thinnest layer possible is 100 µm. The thickest is around 10mm.

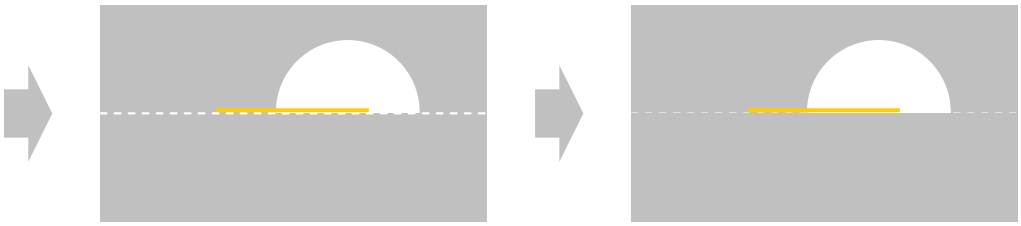
2.6 Integrated electrodes

Metal electrodes may be integrated in glass microfluidic chips. A wide variety of geometries can be created such as interdigitated electrodes, heaters and temperature sensors. The diagram below shows the basic process for electrode fabrication:



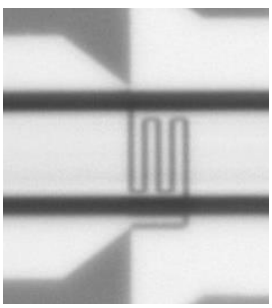
The photoresist layer is removed to expose glass areas. Metal is then deposited on the wafer as shown below:

The photoresist layer is then removed and the chip is sealed using an etched top layer as shown:

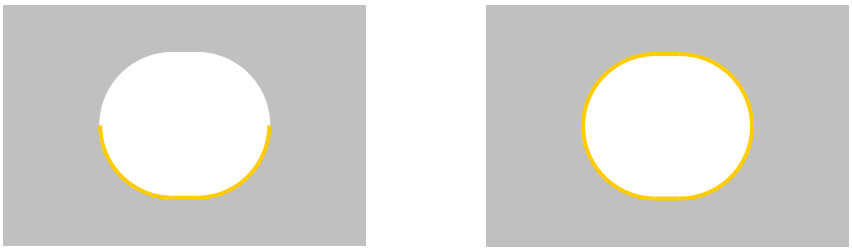


The metal layer that is deposited on the glass surface is normally between 50nm and 1μm in thickness. Platinum is deposited most frequently as it has excellent chemical and heat resistant properties. A wide range of metals can be deposited onto glass including gold. Adhesion of the metal layer to the glass surface is validated using a standard tape test.

Minimum feature size for metal features is 2μm. The image below shows a 2μm wide metal feature inside a 25μm wide channel.



Connections to metal layers are made via holes or by taking the tracks out to the edge of the chip. Metal layers can also be deposited on the inside surface of channels as shown below:



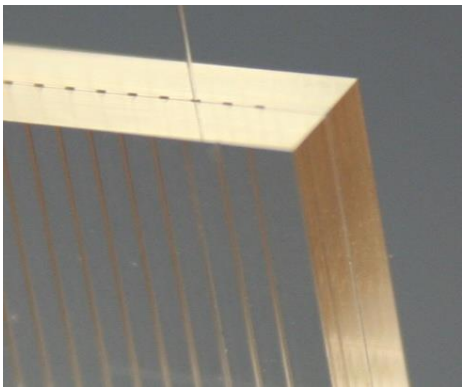
Applications for this type of metal deposition include:

- Optical flow cells – The metal layer can act as an optical light guide or as a mirror allowing reflection of a light beam.
- Catalytic reaction chips – The metal surface can be used to promote chemical reactions

The image below shows a reaction channel with an internal platinum coating

2.7 Dicing

Dicing a wafer of chips produces very clean edges that have a very flat surface finish as shown below:



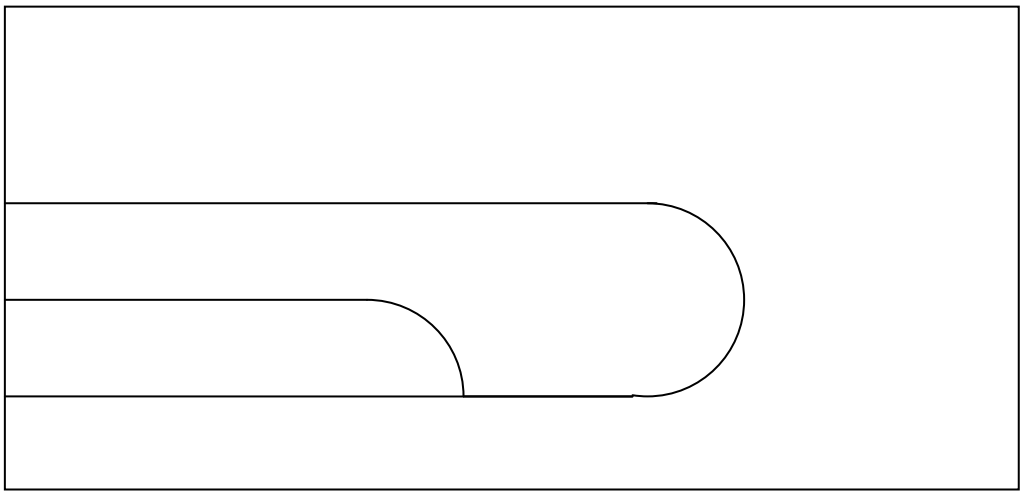
4mm thick glass microfluidic chip

As shown in the diagram above the channels break out through the edge of the chip rather than the top. This allows fluidic and optical connections to be made to the edge of the chip.

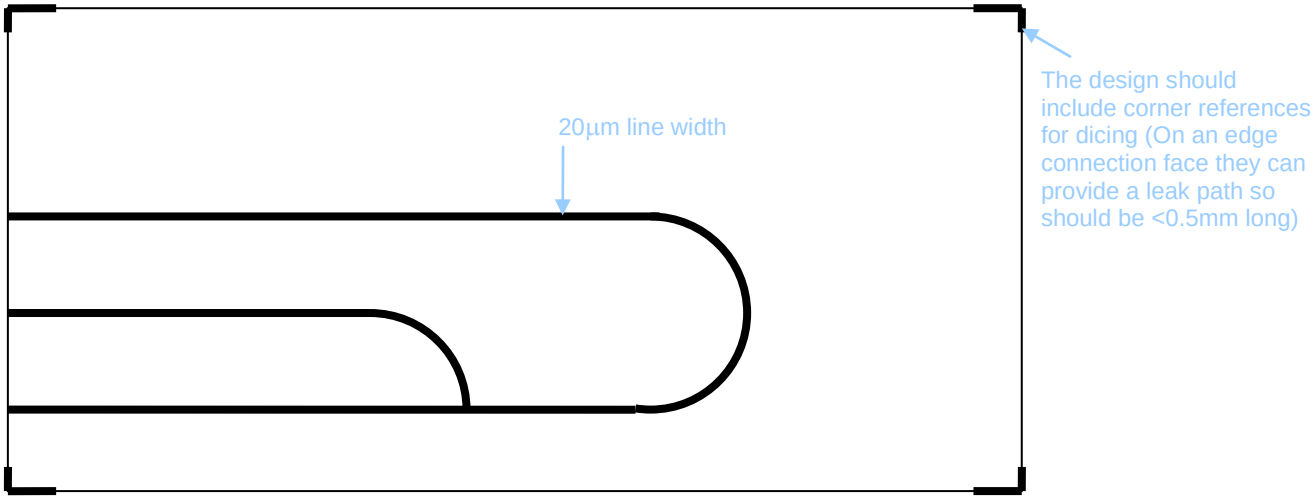
3 Device design guide

3.1 Designing with lines

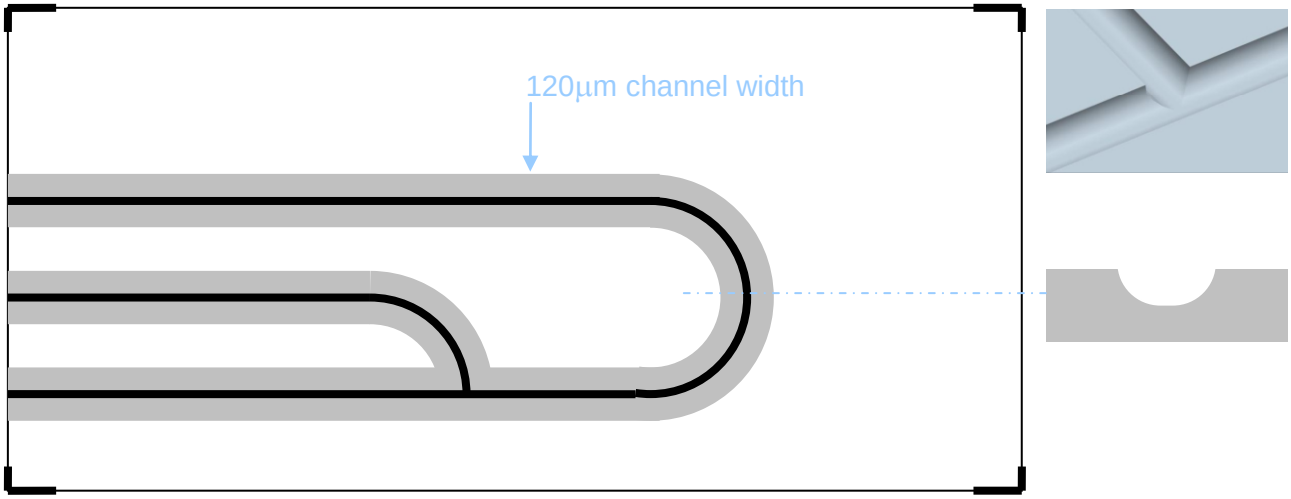
Lines can be used to define the centre of a channel. The diagram below shows a typical CAD image with some sketched lines.



In Dolomite's mask generation process the lines are given a width as shown below:

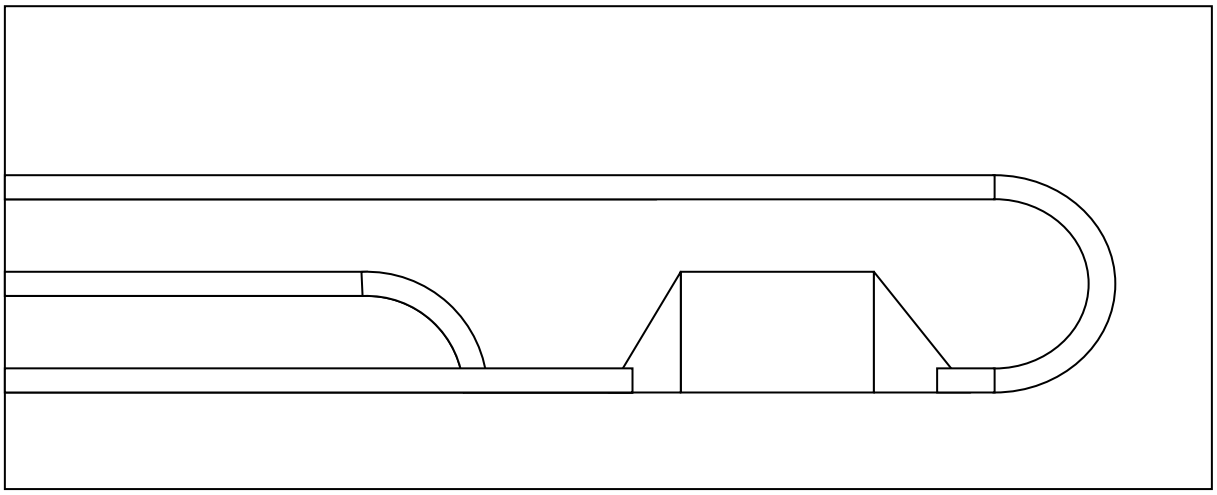


The lines are then isotropically etched to a depth, for example, 50 µm as shown below:

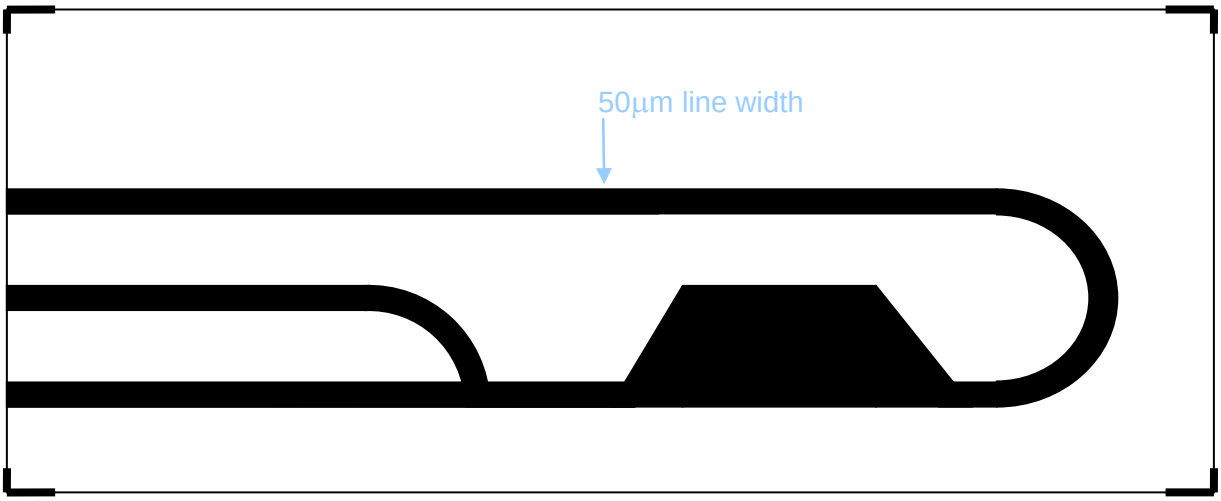


3.2 Designing with polygons

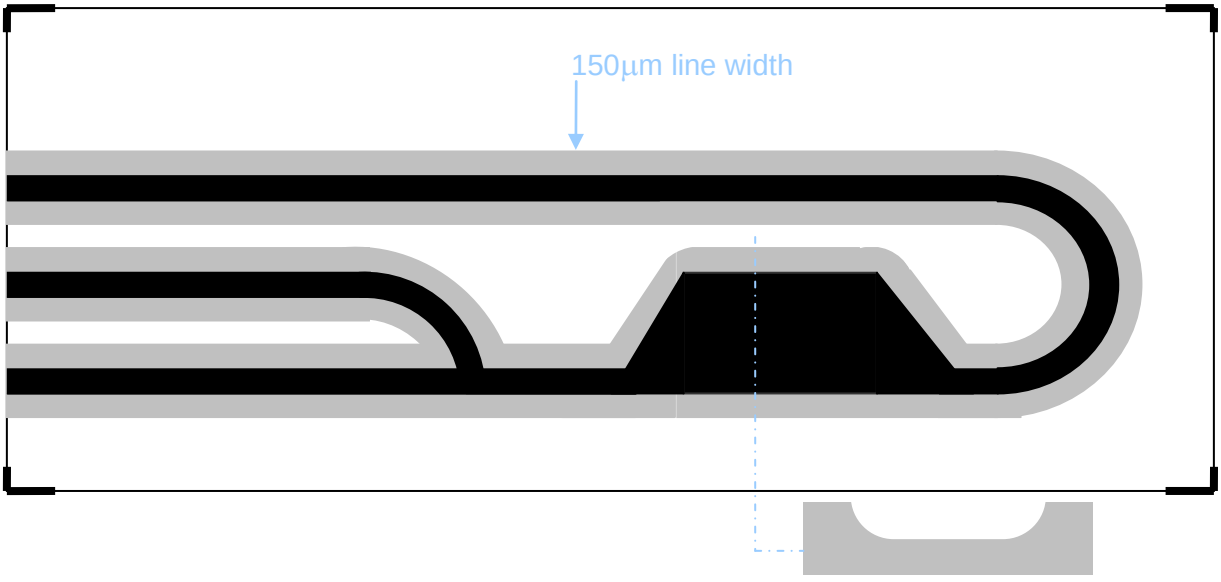
Polygons can be used to define the etched region. It is important that all polygons are closed, otherwise the mask generation process will not work correctly.



In the mask generation process the polygons will be filled as shown below:

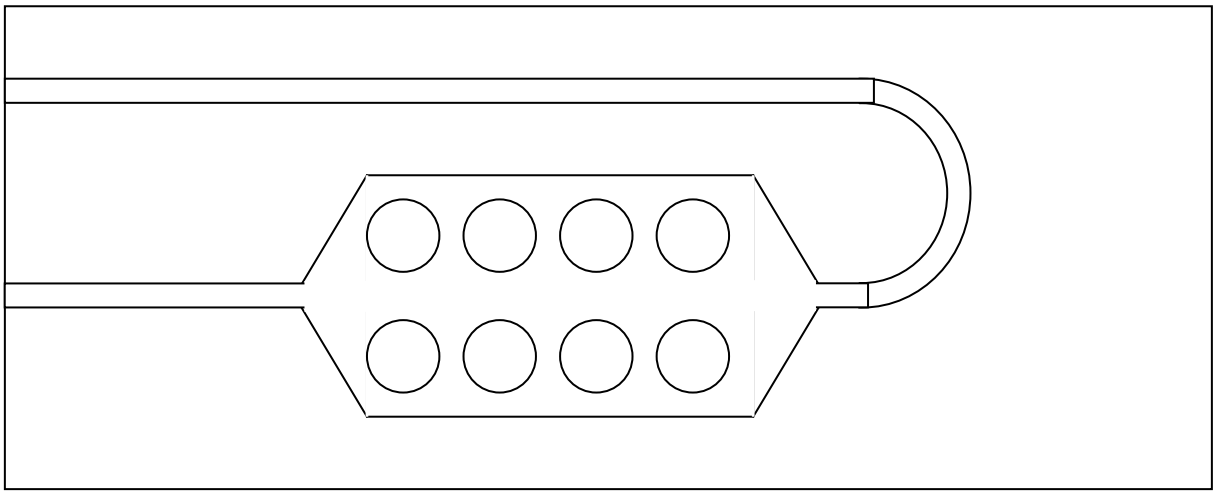


The polygons are then isotropically etched to a depth of 50µm as shown below:

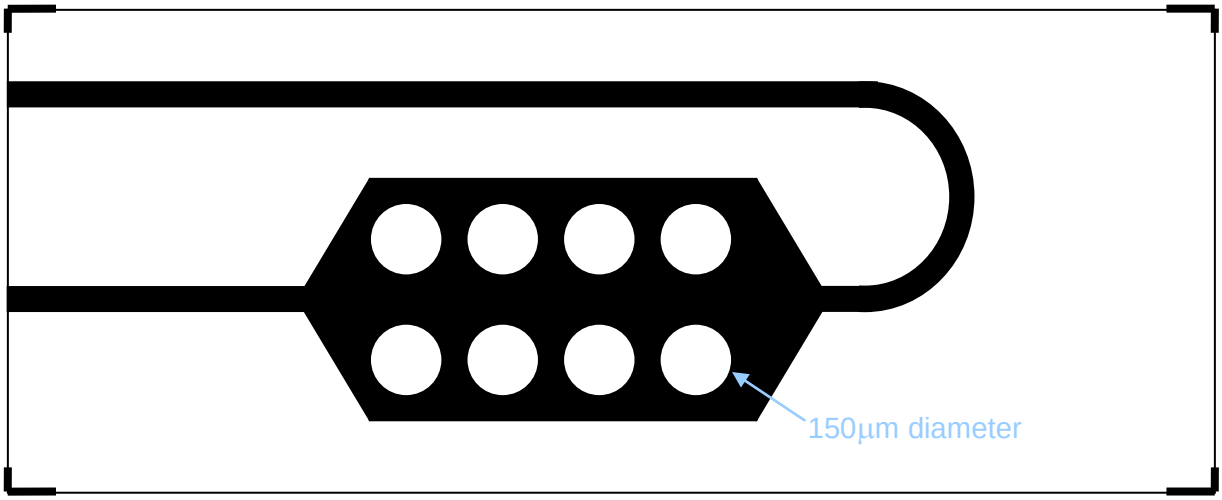


3.3 Creating raised features

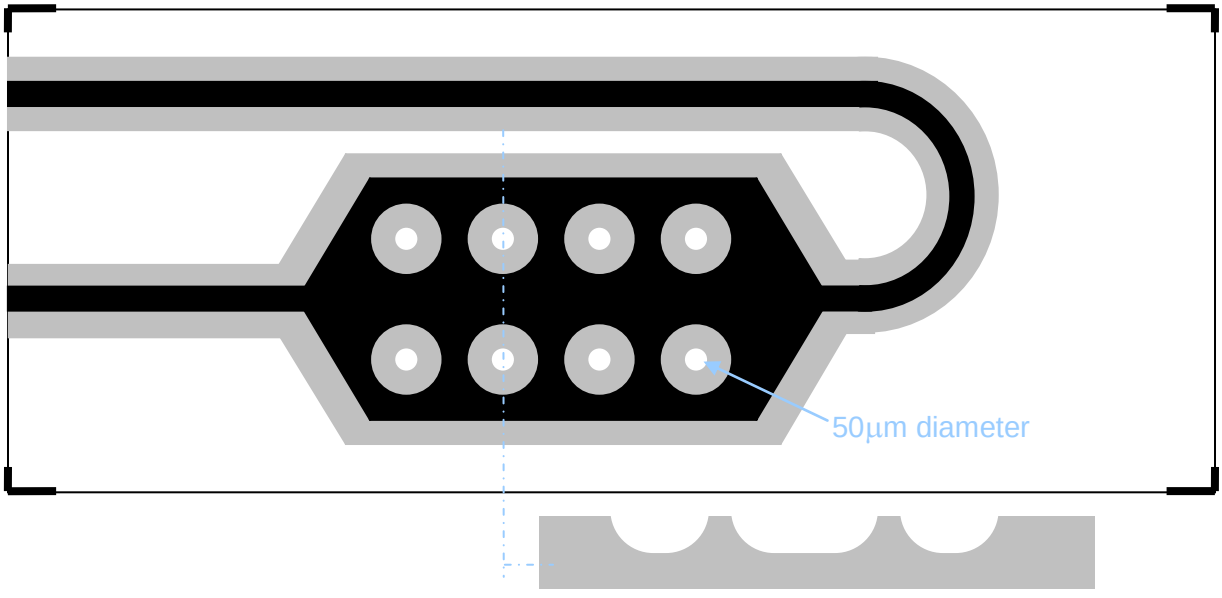
Raised features can be sketched inside etched polygons as shown below:



During the mask generation process the raised features will appear as shown below:

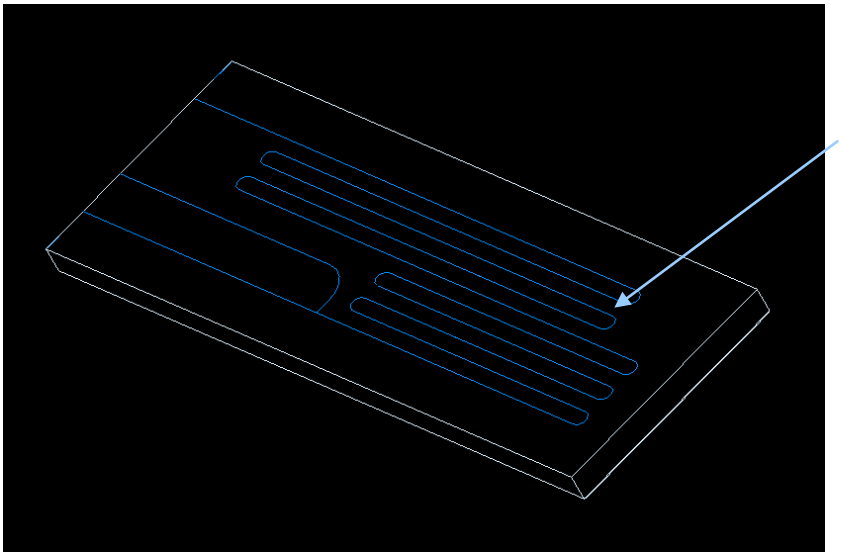


Isotropic etching to a depth 50µm results in size reduction of the raised features as shown below:



4 Drawing file format

Drawing files from a number of different CAD programs can be used to generate the mask pattern for etching. Our preferred formats are DXF or IGES (IGS) file format. These files can be exported from most CAD systems as shown below:



We can also accept DWG files, Bitmap files, GDSII and Gerber.

4.1 Rules for DXF or DWG wafer designs

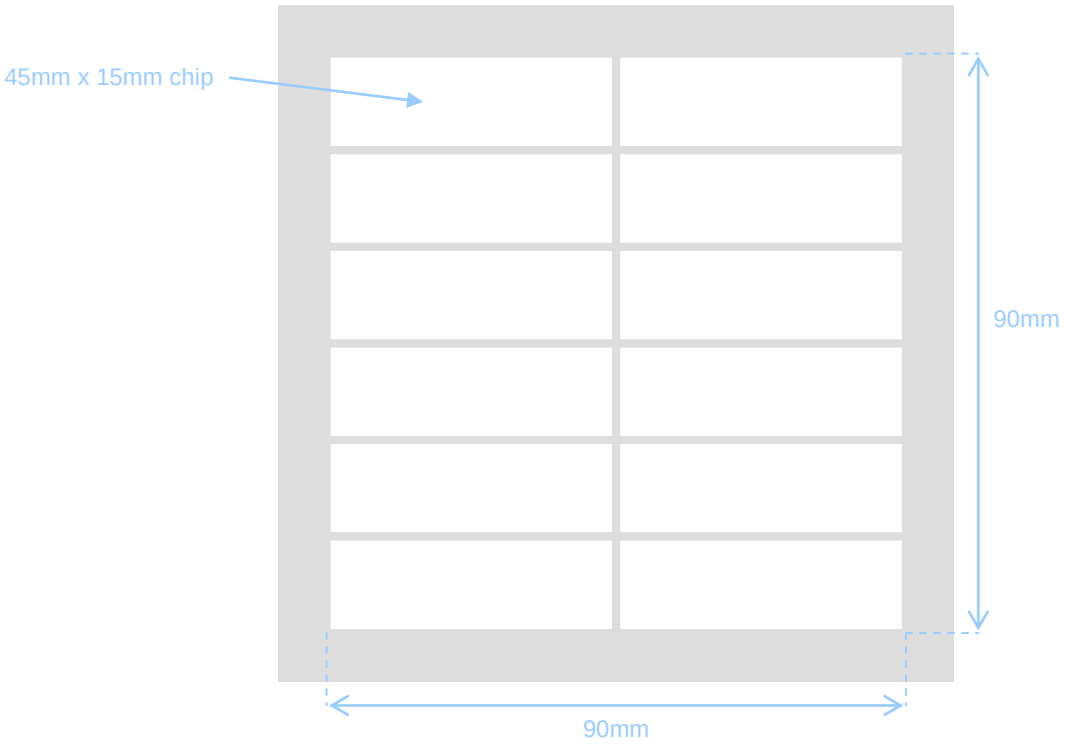
If you are planning to supply Dolomite with a full wafer design (exported from AutoCAD or similar) then it often does not make sense for Dolomite to redraw the channel geometry. In this case it is important to follow the rules set out below when designing the wafer:

1. The channel width in the drawing file should be set so that it equals the line width required for the mask, allowing for widening as a result of the isotropic etching process. If this is not done then the resulting channels will be too wide. If you are unsure then set the line width to zero and use layers as described in point 3 below.
2. When drawing polygon features allow for widening as a result of the isotropic etching process.

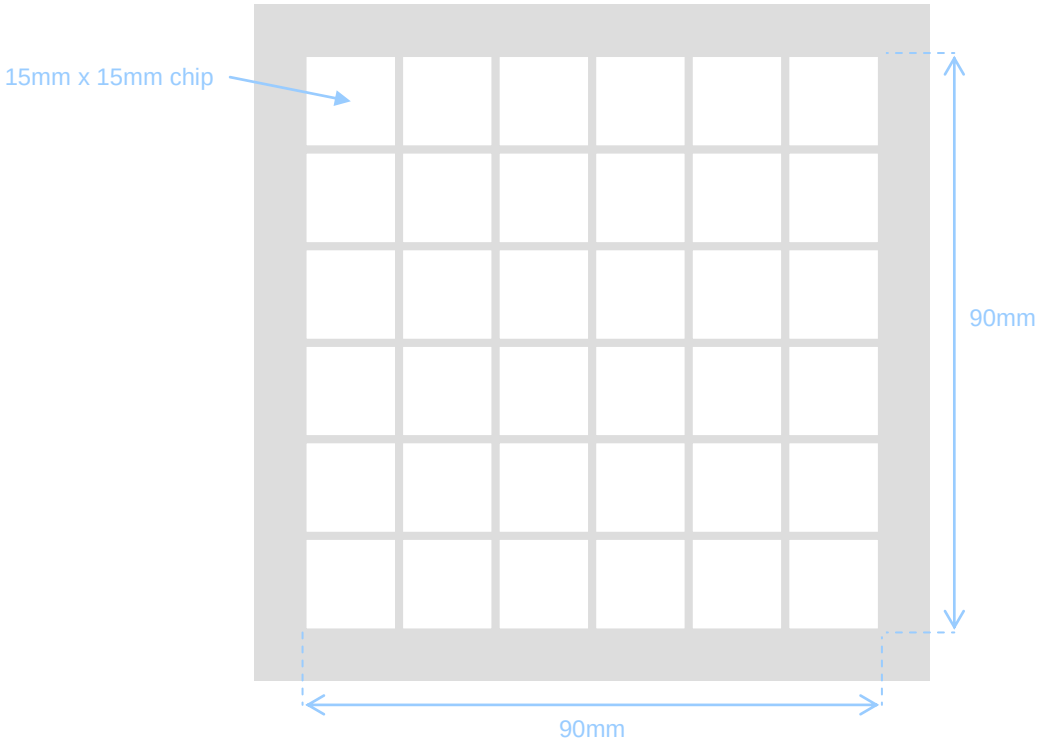
   The exception to 1 and 2 is electrode designs where widening is not an issue.
3. Features should be grouped into different layers in the drawing file. For example all polygons should be in a layer called ‘Polygons’ and all lines which are 10µm wide should be in a layer called 10UM. Separating the features into multiple layers will allow us to make adjustments to the design and edit the layers separately. Please give each layer a name that is easily recognisable. If you are generating lots of chip designs then please be consistent with layer names on each design.
4. OVERLAPPING AND ADJACENT POLYGONS. Please contact Dolomite before creating this kind of design. It may be necessary to take an alternative design approach to save time.
5. Positions of drilled fluid holes or electrode features should be supplied in separate drawing files or in separate layers in the main drawing file. This will allow the geometry data to be extracted for fabrication of tooling or additional masks.
6. Chips should be laid out on the wafer as described in the next section with 0.5mm spacing to allow for dicing saw cuts.
7. Reference lines should be included in the design to indicate the positions of drilled holes and dicing saw cuts. Please contact Dolomite for more information on this as the number of references required will depend on the exact process being used.

4.2 Layout of devices on a wafer

The standard wafer size is 4inch x 4inch which gives a working area of 90mm x 90mm for devices as shown below. A distance of 0.5mm should be left between chips.

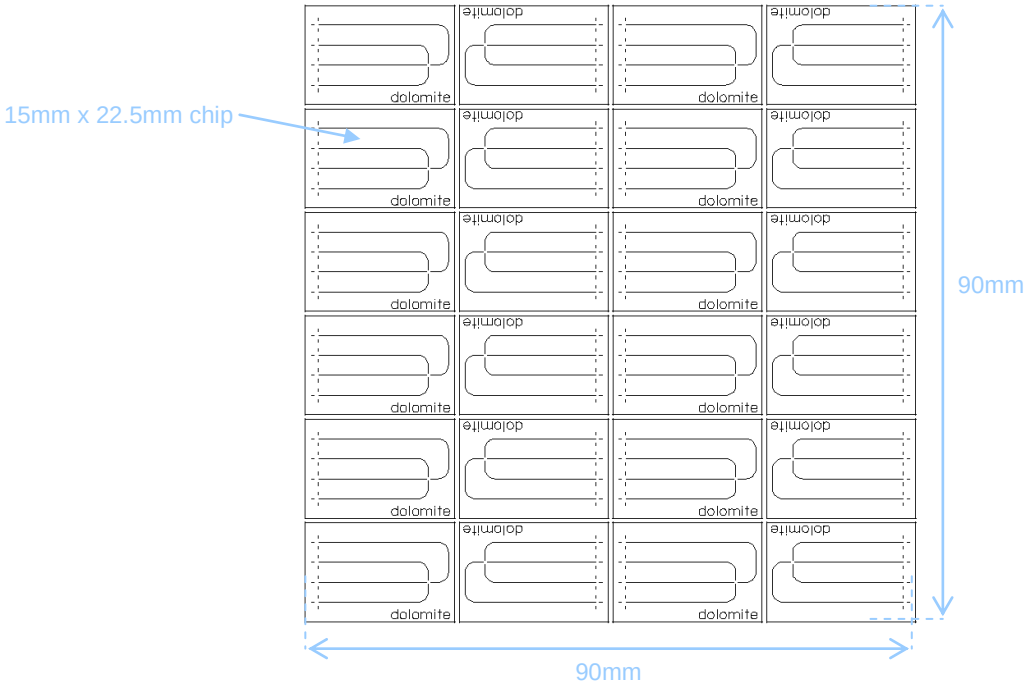


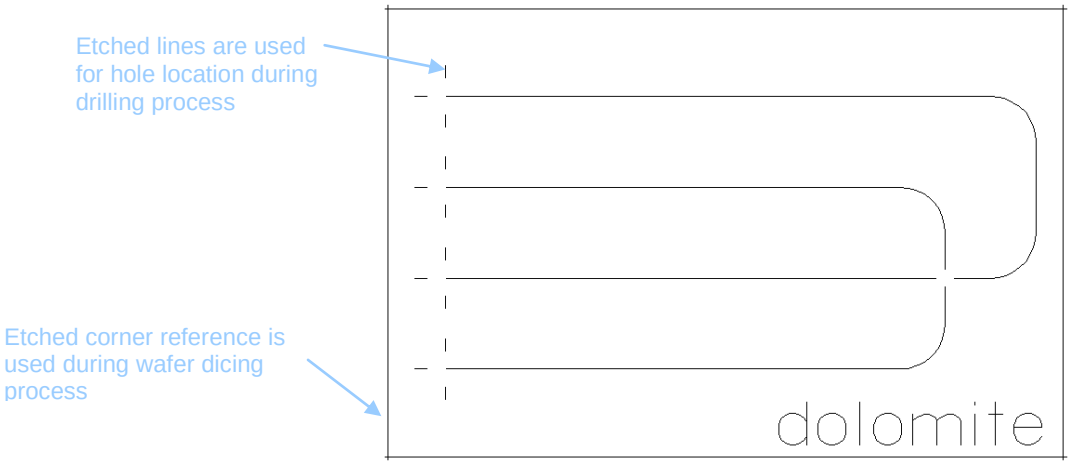
Reducing the footprint of the chips allows more devices to be fabricated from a wafer as shown below:



For chips that are longer than 90mm a 6inch x 6inch wafer can be used.

4.2.1 Example layout

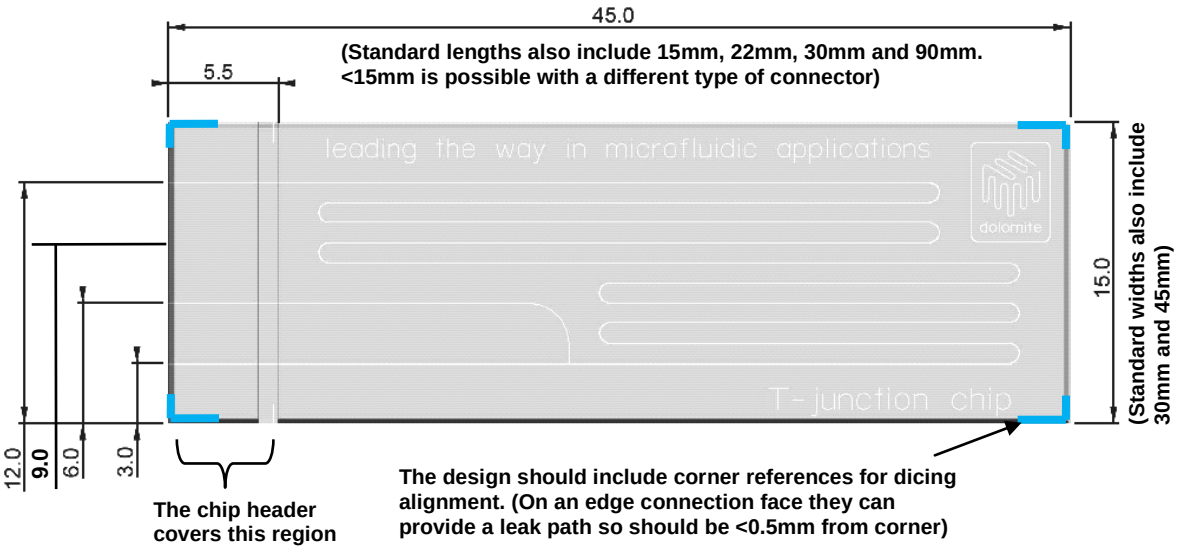




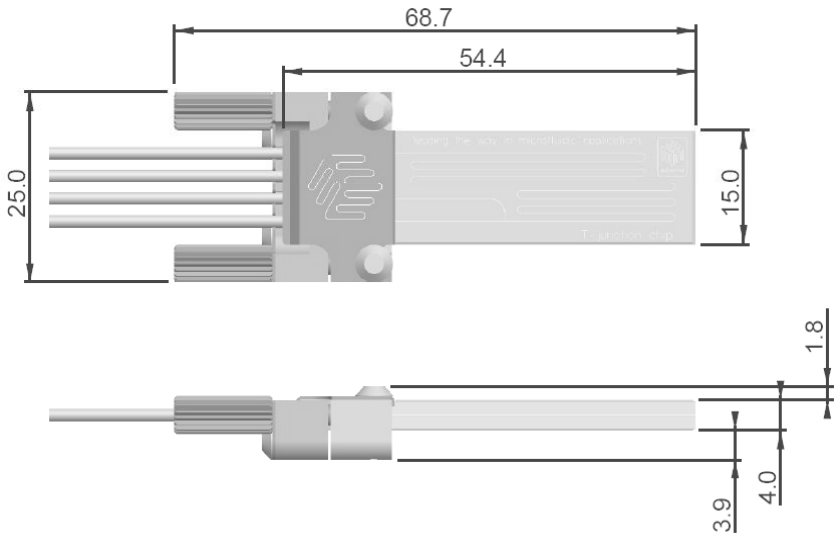
Note: For edge connection the etched corner can create a leak path on the face of the chip that mates with the edge connector. Please check all designs with Dolomite before proceeding with mask fabrication.

4.3 Designing chips with an edge connection

The diagram below shows the layout of a standard T-junction chip. Custom channel layouts can be designed on this format:

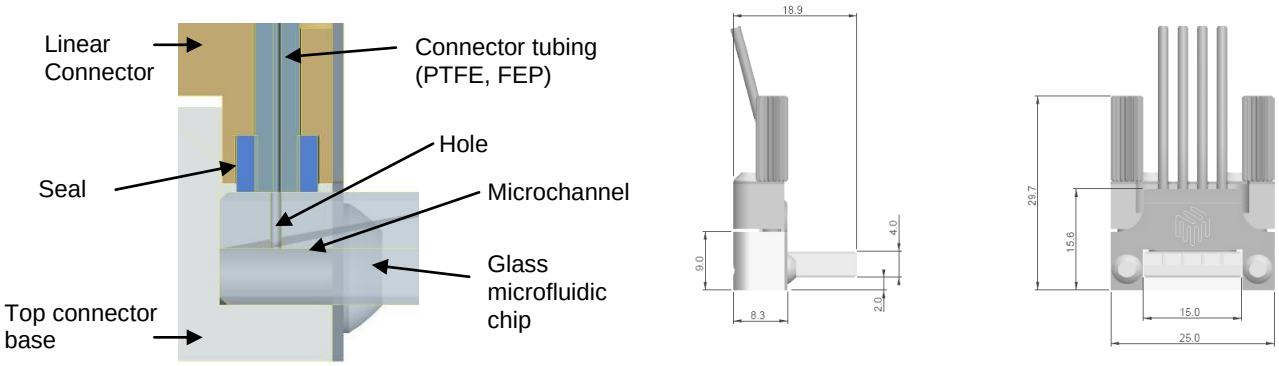


The corner references shown above in blue are required for alignment during the wafer dicing process. If you are designing the whole mask it is important to include these lines so that they are etched into the glass wafer. It is important to make sure these lines do not create a leak path on the face of the chip that will mate with an edge connector. The design team at Dolomite will be able to check this before proceeding with mask manufacture.

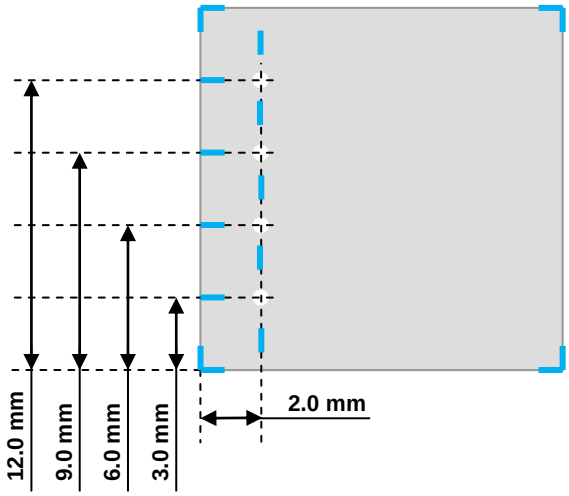


4.4 Designing chips for use with the 4-way linear connector and top connector base

The linear connector can also be used to seal onto the top surface of a chip when used in conjunction with a top connector base. As shown in the diagram below, holes for fluid access are required in the top chip layer.



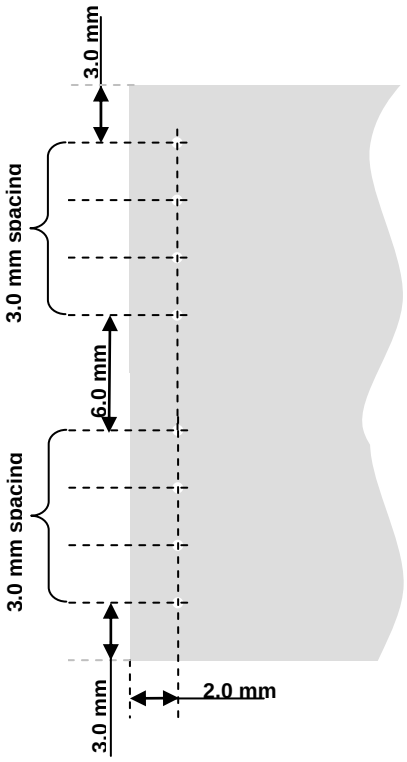
The drilled fluid holes need to be spaced 2mm from the edge of the chip as shown in the layout below:

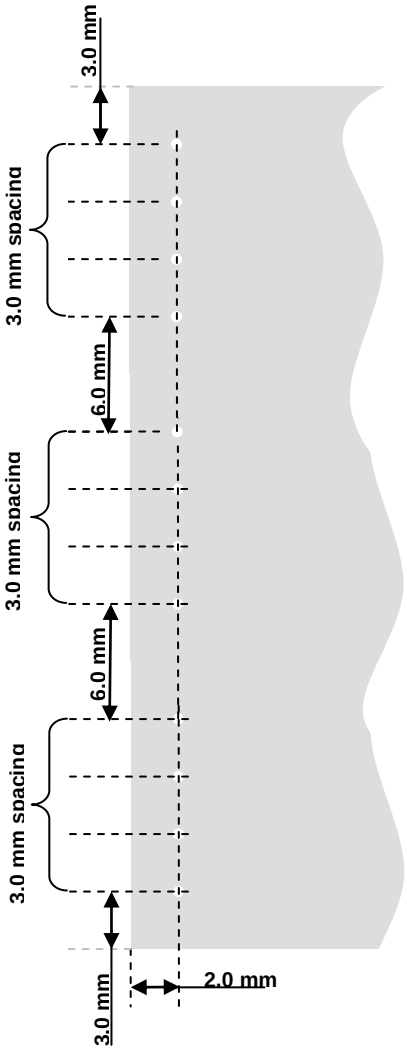


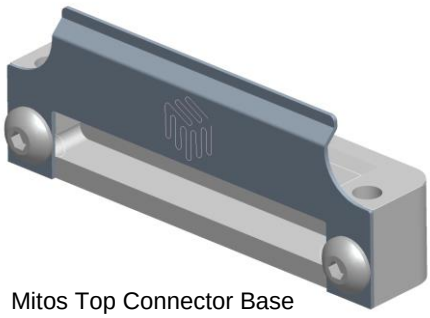
The corner references shown above in blue are required for alignment during the wafer dicing process. If you are designing the whole mask it is important to include these lines so that they are etched into the glass wafer. It may also be necessary to include additional references for hole drilling as shown above. The design team at Dolomite will be able to check this before proceeding with mask manufacture.

4.5 Designing chips for use with the 8-way and 12-way linear connector and top connector base

The images below show plan views of 30mm wide and 45mm wide chips with hole positions. To connect to these chips an 8-way or a 12-way linear connector would be used in combination with the appropriate top connector base. Corner and hole drilling references are not shown in these diagrams.

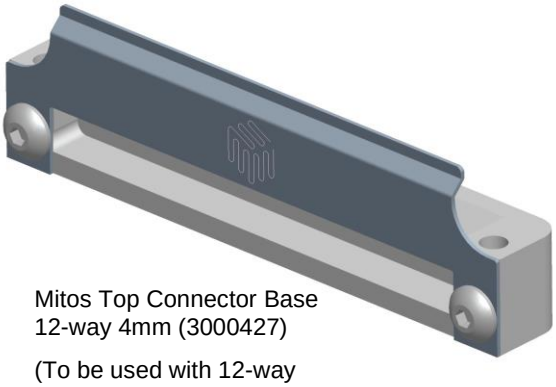






Mitos Top Connector Base 8-way 4mm (3000531)

(To be used with 8-way Linear Connector (3000102))



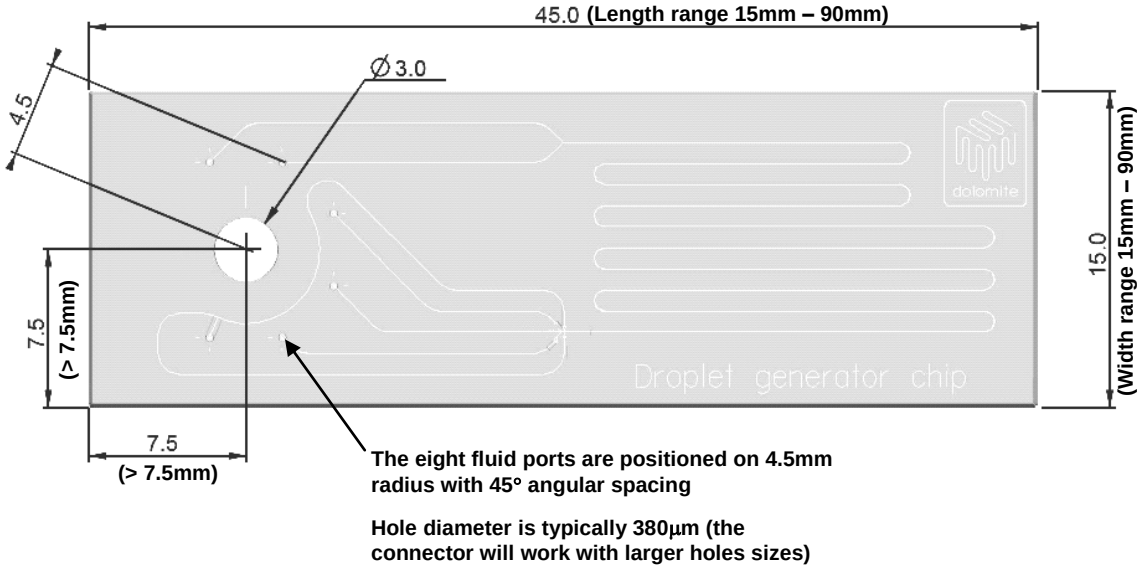
Mitos Top Connector Base 12-way 4mm (3000427)

(To be used with 12-way Linear Connector (3000067))

The two Top Connector Bases shown here work with chips that are 4mm thick. Custom Top Connector Bases can be supplied for thinner chips.

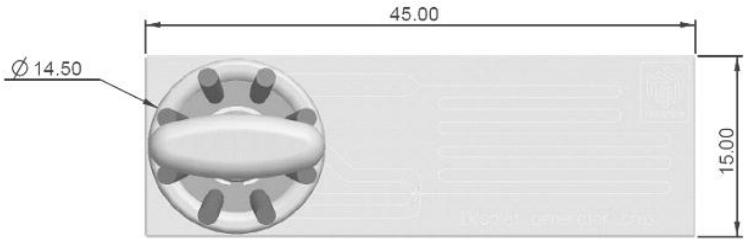
4.6 Designing chips for use with the circular connector

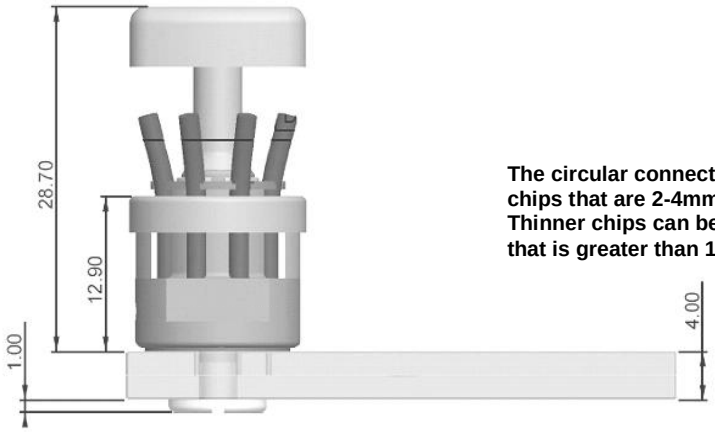
The diagram below shows the layout of a standard droplet generator chip. Custom channel layouts can be designed on this format:



The eight fluid ports are positioned on 4.5mm radius with 45° angular spacing

Hole diameter is typically 380µm (the connector will work with larger holes sizes)





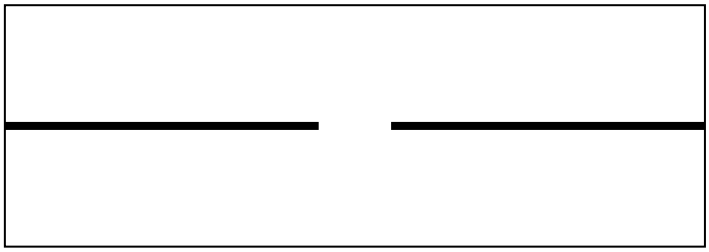
The circular connector will work with chips that are 2-4mm in thickness. Thinner chips can be used with a spacer that is greater than 12mm in diameter.

The corner references and hole drilling references are required for alignment during the wafer dicing process and drilling process. If you are designing the whole mask it is important to include these references so that they are etched into the glass wafer. The design team at Dolomite will be able to check this before proceeding with mask manufacture.

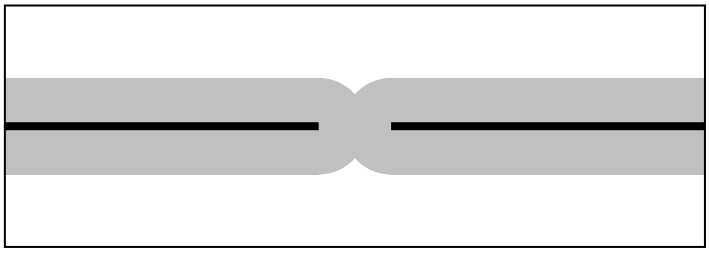
Design examples

4.7 Channel constriction

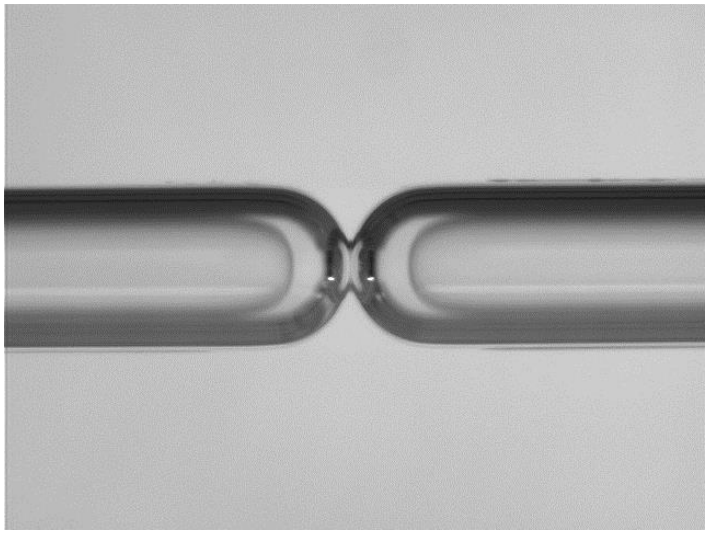
Leaving a gap in the mask line, as shown below, will produce a constriction in a channel:



The gap needs to be < 2 x (etch depth) to ensure that the channel will merge and produce a constriction as shown below:



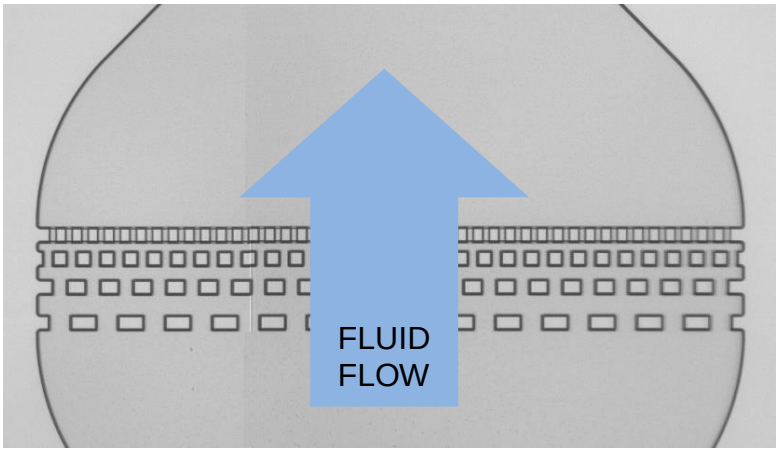
A photo of a real example of this is shown below:



This type of constriction has several applications including the trapping of beads inside a microfluidic device.

4.8 On-chip filter

For small channels (<100µm) it is often useful to include on-chip filters near to the input ports to capture particulate that is accidentally injected into the chip. The image below shows an example of an on-chip filter:



The channel depth in the image above is 14µm and the filter has a total width of 1500µm. The width was chosen to prevent the filter restricting the fluid flow and also to prevent it blocking up quickly.